**Ic Project Second semester 2024-2025**

This project aims to **design, simulate, and analyze a highly efficient, low-power master-slave D flip-flop using Gate Diffusion Input (GDI) logic, implemented in a 32nm (or smaller )CMOS** process. The design leverages the GDI technique to minimize transistor count, reduce power consumption, and decrease propagation delay compared to conventional CMOS flip-flops.

**Objectives:**

* Develop a transistor-level schematic of a GDI-based master-slave D flip-flop.
* Implement the design using Electric EDA -Electric tools and simulate its performance with LTspice.
* Compare the GDI design’s power, delay, and area with a standard CMOS flip-flop.
* Explore adaptive clock generation and body biasing for further power savings.
* Prepare a technical report and presentation summarizing the design process, simulation results, and comparative analysis.

**Expected Outcomes:**

* A validated schematic and layout of the GDI D flip-flop in Electric EDA.
* Simulation waveforms, power, and delay measurements.
* Comparative charts and tables highlighting improvements over CMOS.
* A final report and presentation suitable for IEEE journal submission or academic assessment.

**Deliverables**

* **Transistor-level schematic and layout files** (Electric EDA)
* **Simulation files and results** (LTspice)
* **Comparative analysis** (charts/tables)
* **Final written report** (PDF/Word)
* **Presentation slides** (PowerPoint/PDF)

**Milestone Summary**

* **Schematic and simulation complete**
* **Layout and verification complete**
* **Draft report and slides**